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Substitute for form 1449B/PTO

Complete if Known

(use as many sheets as necessary)

Sheet

2

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Application Number

09/812.030

Filing Date

March 19, 2001

First Named Inventor

Rong Lin

Group Art Unit

Unknown

Examiner Name

Unknown

Attorney Docket Number

87687.042301/R-1265-125

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

[illegible]

**Examiner
Signature**

Date _____

Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.

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03/19/01

Substitute for form 1449A/PTO <h1>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</h1> <i>(use as many sheets as necessary)</i>				Complete if Known	
Application Number				TBA	
Filing Date				Herewith	
First Named Inventor				Rong Lin	
Group Art Unit				Unknown — 2124	
Examiner Name				Unknown — Chat Do	
Attorney Docket Number				87687.042301/R-1265-125	
Sheet	1	of	2		

[illegible][illegible]

Examiner Signature		Date Considered	2/10/04
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Substitute for form 1449B/PTO			Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Application Number	TBA
			Filing Date	Herewith
			First Named Inventor	Rong Lin
			Group Art Unit	Unknown <i>5124</i>
			Examiner Name	Unknown <i>Chaf Do</i>
			Attorney Docket Number	87687.042301/R-1265-125
Sheet	2	of	2	

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
CD	4	Lin, Rong, "A Low-Power Regularly Structured Parallel Multiplier Design", Department of Computer Science, SUNY at Geneseo, Geneseo, NY 14454, pp. 1-11, (March 2000).	
CD	5	Lin, Rong, "A Reconfigurable Low-Power High-Performance Matrix Multiplier Design", Department of Computer Science, SUNY - Geneseo, Geneseo, NY 14454, pp. 1-11, (March 2000).	
CD	6	Lin, Rong, et al, "A Novel Approach for CMOS Parallel Counter Design", Department of Computer Science, SUNY at Geneseo, Geneseo, NY 14454, pp. 1-8, (March 2000).	
CD	7	Lin, Rong, "New Circuits for a Regularly Structured Parallel Multiplier Design", Department of Computer Science, SUNY - Geneseo, Geneseo, NY 14454, pp. 1-19, (June 24, 1999).	
CD	8	Lin, Rong, "Reconfigurable Buses With Shift Switching -- VLSI Radix Sort", 1992 International Conference on Parallel Processing, CRC Press, Boca Raton, pp. III-2 - III-9, (August 17-21, 1992).	
CD	9	Lin, Rong, "Shift Switching and Novel Arithmetic Schemes", IEEE Proceeding of ASILOMAR-29, pp. 580-585, (1996).	
CD	10	Ling, Rong, et al., "Reconfigurable Buses With Shift Switching: Concepts and Applications", IEEE Transactions on Parallel and Distributed Systems, Vol. 6, No. 1, pp. 93-102, (January 1995).	
CD	11	Lin, Rong, et al., "Efficient VLSI Architectures for Columnsort", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 7, No. 1, pp. 135-139, (March 1999).	

Examiner Signature		Date Considered	2/10/04
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